In The Claims

Applicant is amending the claims in this application under 37 CFR 1.111 and 37 CFR 1.121.

Please cancel claims 4, 5, 9, 10, 14, 15, 19, and 20 as shown in this amendment.

Please amend claims 1-3, 6-8, 11-13, and 16-18 as shown in this amendment.

Following is the currently pending claims in clean form on separate pages with parenthetical statements that show the claim being amended, canceled, newly added, or left unchanged.

Additionally, included with this amendment is a version with markings to show the changes made to the currently pending claims as amended and the claims as originally filed.

Additionally, included with this amendment, for the Examiner's convenience, is a clean version of the currently pending claims as amended without parenthetical statements.

CLAIMS

We claim the following invention:

1. (First Amended) A signal model used in an N-NARY logic simulation, comprising:

a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

2. (First Amended) The model of Claim 1, wherein said logic value further comprises an integer less than or equal to 31.

3. (First Amended) The model of Claim 1, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

4. Canceled.

5. Canceled.

6. (First Amended) A method that makes a signal model used in an N-NARY logic simulation, comprising:

assigning a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

assigning a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

assigning a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

7. (First Amended) The method of Claim 6, wherein said logic value further comprises an integer less than or equal to 31.

8. (First Amended) The method of Claim 6, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

9. Canceled.

10. Canceled.

11. (First Amended) A method that uses a signal model used in an N-NARY logic simulation, comprising:

reading a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

reading a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled;

reading a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled; and

providing said signal value, said signal state, and said signal definition to the software-implemented simulation of the N-NARY logic design.

12. (First Amended) The method of Claim 11, wherein said logic value further comprises an integer less than or equal to 31.

13. (First Amended) The method of Claim 11, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

14. Canceled.

15. Canceled.

16. (First Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method that uses a signal model used in an N-NARY logic simulation, comprising:

reading a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

reading a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled;

reading a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled; and

providing said signal value, said signal state, and said signal definition to the software-implemented simulation of the N-NARY logic design.

17. (First Amended) The program storage device of Claim 16, wherein said logic value further comprises an integer less than or equal to 31.

18. (First Amended) The program storage device of Claim 16, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

19. Canceled.

20. Canceled.

21. (First Amended) A signal modelling system used in an N-NARY logic simulation, comprising:

a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

22. (First Amended) The system of Claim 21, wherein said logic value further comprises an integer less than or equal to 31.

23. (First Amended) The system of Claim 21, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

24. Canceled.

25. Canceled.